

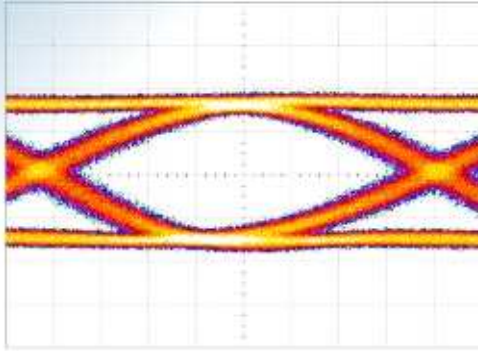


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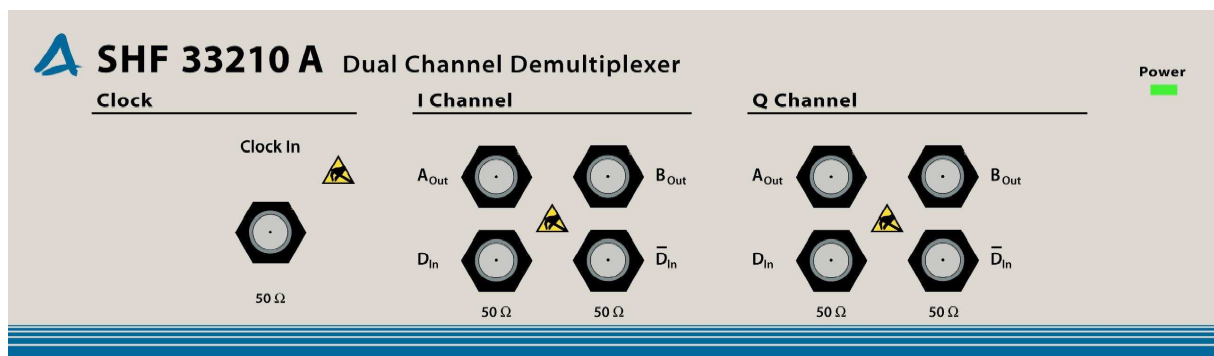
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Datasheet

SHF 33210A

28 Gbps Dual Channel 1:2 Demultiplexer





Description

The SHF 33210A dual channel demultiplexer consists of two 1:2 demultiplexers driven from a common clock source. It generates four output data streams (e.g. 4 x 14 Gbps) of half of the input data rate from two input data signals (e.g. 2 x 28 Gbps). It is a field replaceable plug-in module which needs to be installed in a mainframe type SHF 10001A or SHF 10000B. Together with other plug-in modules from this instrument series, a modular and scalable measurement system can be configured.

The mainframe with the installed modules is controlled over a standard Ethernet connection by an external computer which is a standard part of the package. An easy to use software package provides not only a user friendly interface for changing the operating parameters but also the capabilities of feature enhancement through firmware & software upgrades

Broadband operation capabilities of up to 28 Gbps input data rate are given by the architecture of the instrument. The demultiplexer excels by a very good input sensitivity and facilitates easy testing of ultra high speed components and their assembly into complex communication systems.

A single master clock signal of half the input data rate is used to drive the two demultiplexers. To align the phase of the clock with respect to the input data for each demultiplexer individually, two motor controlled delay lines are installed inside the instrument.

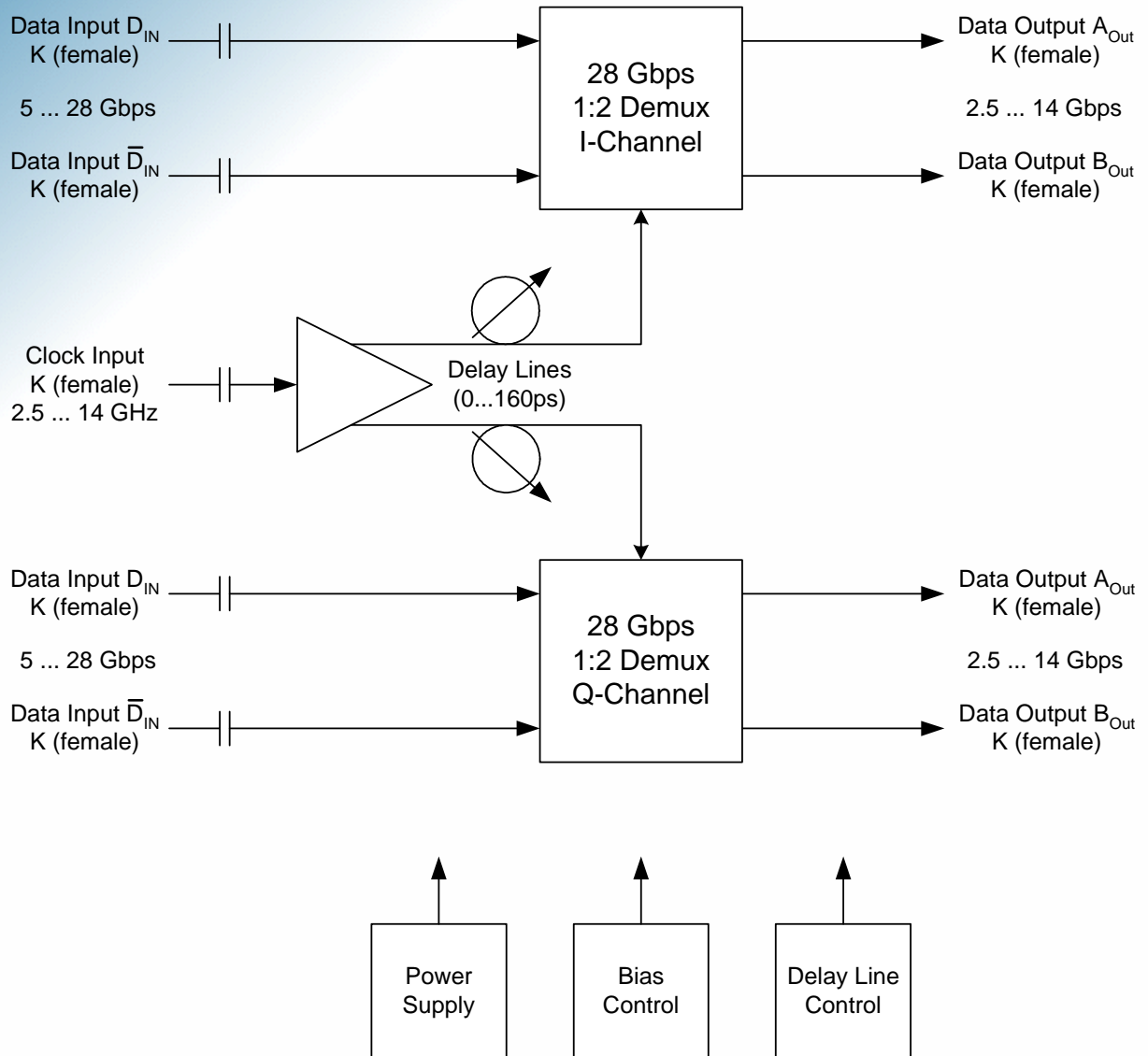
The SHF 33210A dual channel demultiplexer is a result of SHFs many years experience in the development and production of ultra high speed components and their assembly to more complex systems.

Features

- Scalable and modular system
- Broadband operation 5...28 Gbps (input bit rate)
- Windows Style Bert Control Center software package
- Computer controlled operation over Ethernet which also enables remote access
- Feature enhancement through firmware & software upgrades
- High precision 2.92mm female (K compatible) connectors for all inputs and outputs
- External master clock input at half of the input bit rate
- High precision motor controlled delay lines to adjust the clock phase
- Excellent input sensitivity



Functional Block Diagram



Specifications

Parameter	Unit	Min.	Typ.	Max.	Conditions
Clock input (AC coupled)					
Connector type			50 Ω		2.92mm female (K compatible) connector
Frequency range	GHz	2.5		14	half bit rate
S11	dB			-10	
Input level	V_{pp}	0.4		0.8	AC coupled
Clock delay range	ps	0		160	in 1 ps steps

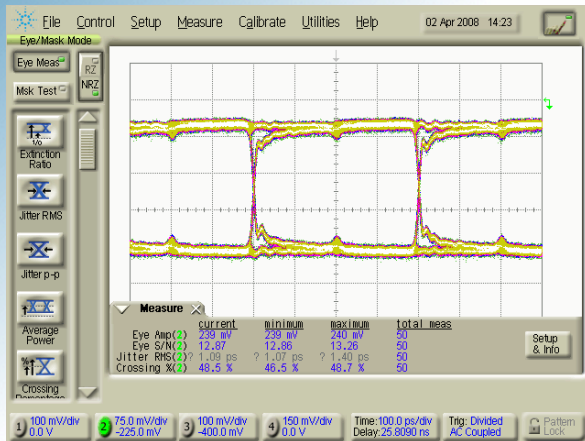


Parameter	Unit	Min.	Typ.	Max.	Conditions
Data inputs (AC coupled)					
Connector type			50 Ω		2.92mm female (K compatible) connector
Bit rate	Gbps	5		28	
S11	dB			-10	
Sensitivity	mV			50	Eye Height, BER 10^{-9}
Clock phase margin	$^{\circ}$	200			
Input Level	mV _{pp}	50		800	
Data outputs (DC coupled, Ground referenced CML)					
Connector type			50 Ω		2.92mm female (K compatible) connector
Bit rate	Gbps	2.5		14	
Output level	mV _{amp}	200			
Rise/fall time	ps			30	20%...80%
General					
Power consumption	W		20		
Weight	kg		2.9		
Dimensions (WxHxD)	mm	445x215x60			
Operating temperature	$^{\circ}\text{C}$	10		35	
Storage temperature	$^{\circ}\text{C}$	-20		70	

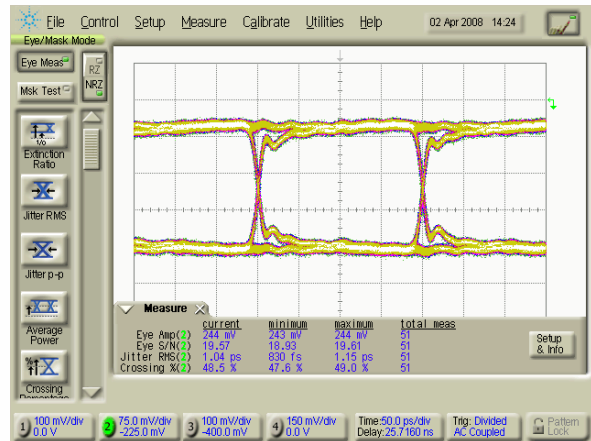


Output Waveforms

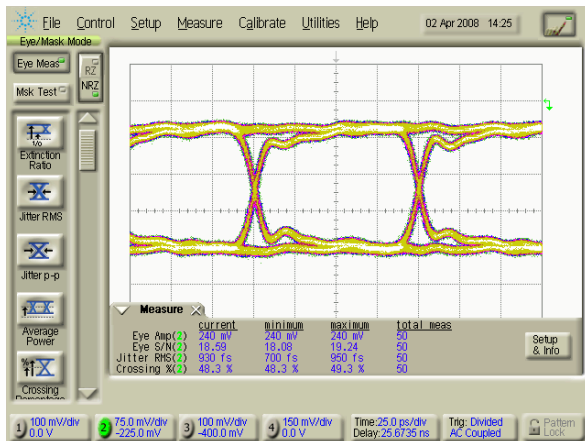
Typical Output Signal Waveforms, PRBS 2³¹-1



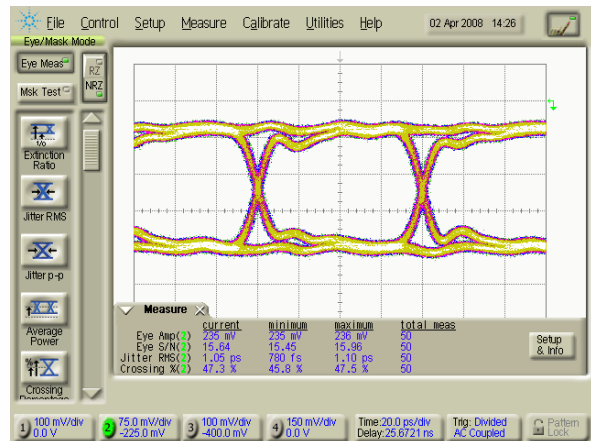
5 Gbps Input Bit Rate



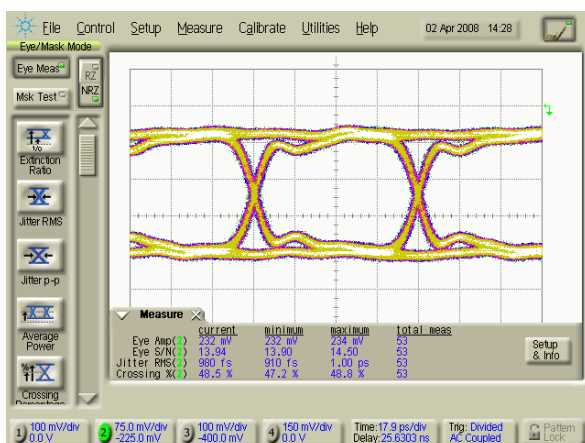
10 Gbps Input Bit Rate



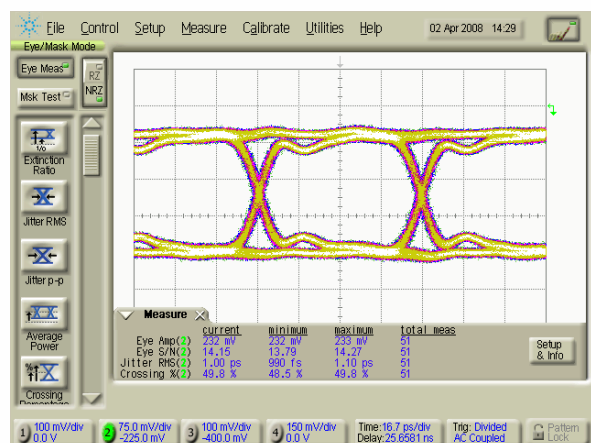
20 Gbps Input Bit Rate



25 Gbps Input Bit Rate



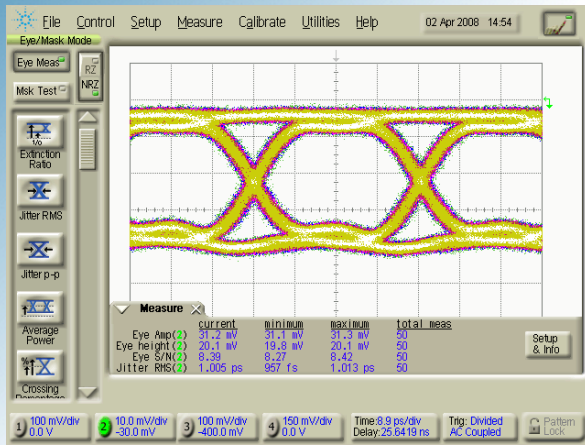
28 Gbps Input Bit Rate



30 Gbps Input Bit Rate



Minimum Input Signal, PRBS 2³¹-1



28 Gbps, BER < 10⁻⁹