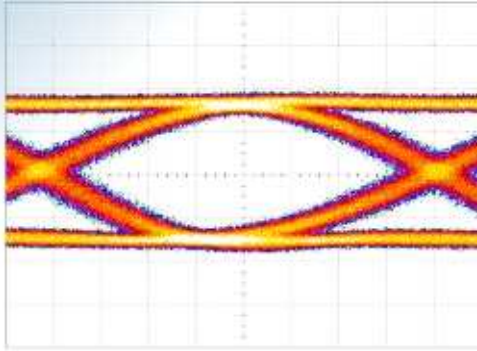




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# Brief description

## PCILWL

### preliminary





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### Contents

1.	Application range .....	3
2.	Functional description .....	3
3.	Size of data packages and data rate .....	3
4.	Data connection .....	4
5.	Service interface .....	4
6.	PCI-connection and board size.....	4



## 1. Application range

The component PCILWL is used for the interconnection of PCs and VME-systems via an optical fiber (OF). The simplest case is a peer-to-peer connection between two systems. There can be a VME-system or a PC alternatively on both sides. The connection of more than two systems is ensured by the use of the component HUB20.

VME-systems and PCs can be combined in any order as long as the sum of 20 systems is not exceeded.

The data exchange between the systems is made in a synchronous manner according to the principle of reflective memory. The synchronous clock is 1ms and given by the master device. The master is one interconnection component if two systems are connected. If a HUB20 is used so this is the master.

## 2. Functional description

Every interconnection component has a dual port RAM (DPR) with a size of 512kByte. One port of the DPR can be accessed from the PCI-bus, the second from the OF-transceiver which is responsible for the data exchange with the other interconnection components.

Certain areas of the DPR are allocated to every interconnection component. Only the component to which these areas are allocated to may write to it. The data of these areas are mirrored to all other interconnection components. In this way all data are available to all components after a short delay.

Four different areas A, B, C and D can be allocated to one component. The areas allocated must not border on each other. They can be positioned in the DPR at any address. But the user has to ensure that the address is divisible by four, e.g. to be a double word address, and no other area in the whole system is overlapping.

The areas A to D are differently prioritized. The prioritization is made by not transmitting the complete areas B to D during a transmission cycle. The complete areas will be transmitted in sections during succeeding transmission cycles. Only the area A is transferred completely during every transmission cycle. In how many sections the areas B to D are divided into is determined by the configuration. The areas B and C can be independently from the other divided into until 255 sections, the area D into until 65535. It is possible to mirror very large memory areas in this way.

## 3. Size of data packages and data rate

The size of the data packages of a connection component is limited to 4096 bytes. 4060 bytes of user data remains after subtracting the protocol overhead. The size of the packages per data cycle need not be constantly because of the transmission in sections of the areas B to D described in chapter 2. An automatic check regarding the compliance of maximum size of data packages is made after configuration. If the maximum size is exceeded a message is sent via the service interface (s. chapter 5). Further more the transmission of data is disabled.



Depending on the configuration and the number of systems connected the maximum data rate is about 12 to 16kByte/ms at receiver side.

#### **4. Data connection**

A multimode optical fiber is used for the data connection. It is operated with 250MBaud fully duplex. A gross data rate of 200MBaud remains because of the 8 to 10bit coding/decoding achieved by the SERDES-devices. SFP-modules are used as transceiver devices.

#### **5. Service interface**

The component PCILWL has a serial service interface led through a DSUB09-connector. Configuration data can be loaded, version numbers polled and error states signaled with the help of it. A usual terminal program running on a PC for instance can be used for this purpose. The parameters of the interface are: 38400kBaud, 8, E, 1.

#### **6. PCI-connection and board size**

The component is achieved as a short 3.3V-board with 32bit-bus according to the PCI specification revision 2.1. The PCI-clock is 33MHz.