

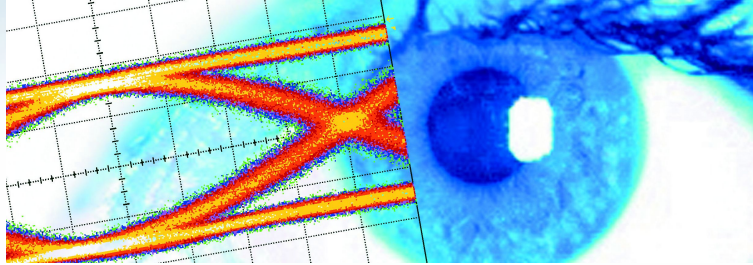


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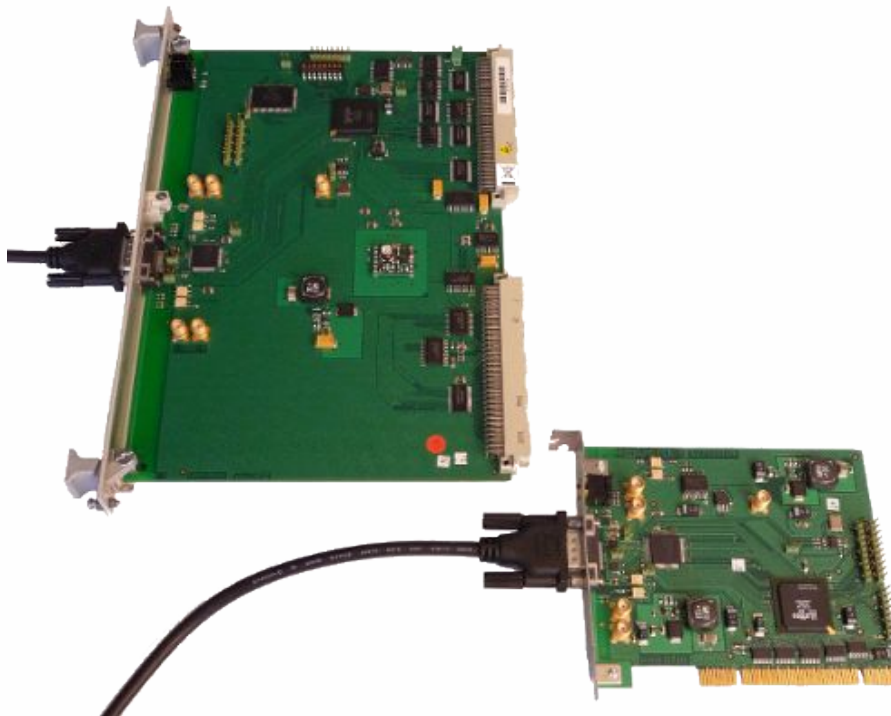
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Manual PCK-PCKV: PCI to VME coupler





Content

1 Overview.....	3
2 Front Panel.....	4
3 Jumper.....	5
4 PCI-VME-Bridge.....	6
4.1 VME Interface.....	6
4.2 Dual-Port-RAM.....	7
5 Link.....	8
5.1 Access FIFO Watermarks.....	8
5.2 Link Test.....	9
6 Register Description.....	10
6.1 PCI Memory and I/O mappings.....	10
6.2 PCI Configuration Register.....	10
6.3 I/O-Register.....	11
6.3.1 Status (0x08)	11
6.3.2 Interface Config (0x10)	12
6.3.3 Test Mode (0x14)	12
6.3.4 Interrupt (0x18)	12
6.3.5 Control (0x1C).....	13
6.3.6 VME Page (0x20)	13
6.3.7 uSec-Timer (0x24)	13
6.3.8 CRC Error counter (0x28)	13
6.3.9 VME CRC Error counter (0x2C).....	14
6.3.10 Test Mode Errors (0x30)	14
6.4 VME Register.....	14
6.4.1 VME Control Register.....	15
6.4.2 VME Status Register (0x04).....	15
6.4.3 Interface Configuration (0x40).....	16
6.4.4 DIP-Switch (0x47).....	16
6.4.5 DPR A32 Address (0x48).....	16
6.4.6 DPR A24 Address (0x4C).....	16
6.4.7 Link Configuration (0x50).....	17
6.4.8 Microseconds Counter (0x54).....	17
6.4.9 Link Status and Test (0x58).....	17
6.4.10 CRC Error Counter (0x5C).....	17
6.4.11 Test Error Counter (0x60).....	18
6.4.12 VME Error Register 1 (0x64).....	18
6.4.13 VME Error Register 2 (0x68).....	18
6.4.14 Access FIFO Error 0 (0x6C).....	18
6.4.15 Access FIFO Error 1 (0x70).....	18
6.4.16 Access FIFO Error 2 (0x74).....	18
6.4.17 Interrupt-Acknowledge (0xE4-0xFF).....	19
6.4.18 RAM (0x100-0x3FF).....	19
7 Drivers.....	19
8 Technical Data.....	20
8.1 PCK.....	20
8.2 PCKV.....	20
9 Environmental Conditions.....	20
10 Ordering Information.....	21



1 Overview

The PCK/PCKV system is a fast connection between PCI and VME bus featuring a direct and transparent access from the PCI to the VME bus via a fast serial link running at 1.4 Gbps.

The VME address space is mapped to the PCI as if the PCI device would have a direct connection to the VME.

The PCKV VME board requires one mounting position (Slot) in the rack. It has 512 KB dual port RAM for data exchange with other VME CPU boards and can operate as a system controller.

The PCKV complies with the VMEbus specification IEEE 1014-1987.

The PCK complies with PCI specification 3.0.

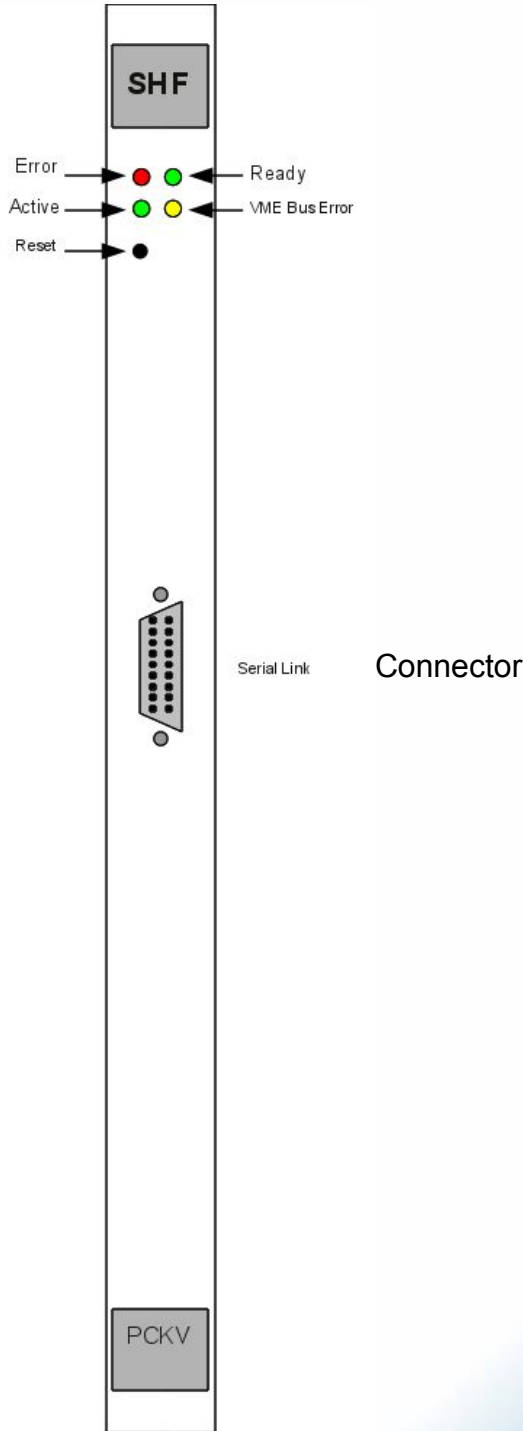
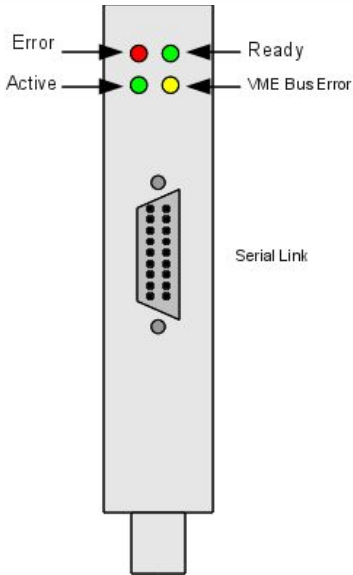
Drivers and application software are available for Windows XP and Linux.



2 Front Panel

4 LEDs, 2 green, yellow, red

Serial Link using PCI Express 1x external

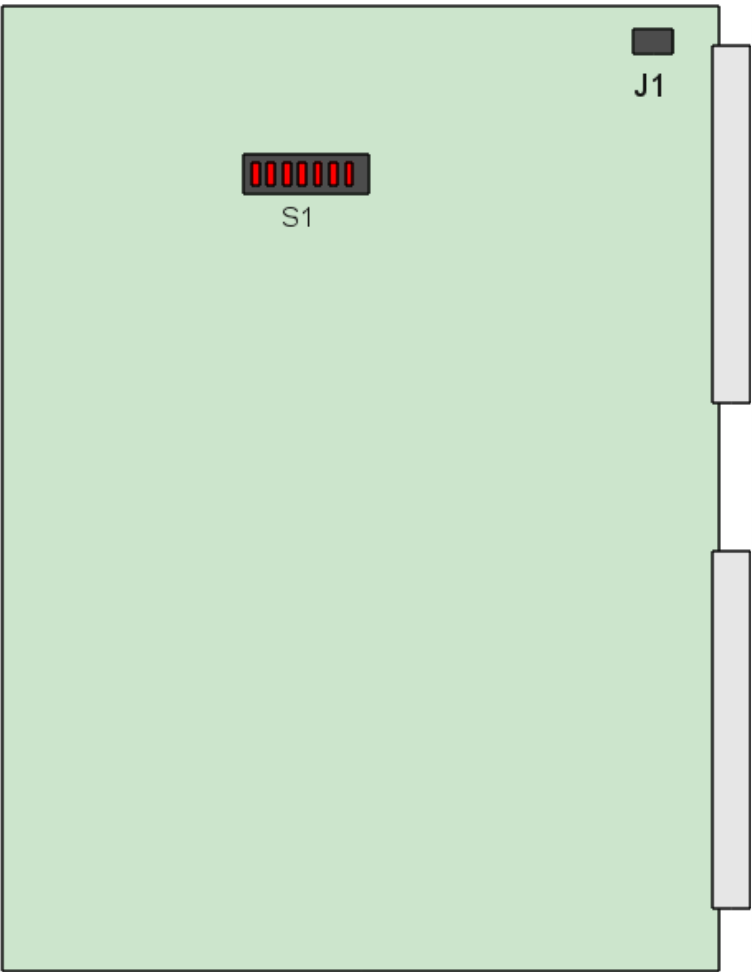




3 Jumper

J1: disable System controller

S1: VME Address for DPR





4 PCI-VME-Bridge

The PCI interface acts as a bridge device to the VME bus and the dual-port-RAM (DPR). It maps the VME A16, A24 and the A32 address space directly to the PCI address space where the A32 space is mapped in two slices at 16, 64 or 256MB each with separate page registers to address the full 32-bit space. The VME registers and the DPR are addressed as VME slaves at their respective address but the local accesses are not forwarded to the VME bus (see details in chapter 10).

Write accesses to the VME are posted and acknowledged immediately to the PCI to improve performance. A configurable FIFO on the VME side can store up to 128 accesses. A read access is delayed on the PCI side until all pending write accesses are performed and the read data has been transferred.

4.1 VME Interface

The VME-bus interface is a master/slave interface supporting A32, A24 and A16 addresses and D8, D16 and D32 data widths. The master's VME address regions for A16 and A24 are mapped directly to the PCI address space of the CPU where the A32 region is assessable via two 16-256 MB mappings with separate page registers to access the full 4 GB range.

Revision 2 of the PCK card has a DIP-Switch to set the size for the A32-areas, revision 1 is always using two regions of 256MB each.

Sw1/3	Sw2/4	A32 size	Page Register Bits used
Off	Off	256 MB	A: 4-7, B: 12-15
On	Off	64 MB	A: 2-7, B: 10-15
Off	On	16 MB	A: 0-7, B: 8-15
On	On	disabled	Not used

Sw1-2 are controlling the first A32-range of PCI Base Register 3 and Page A, Sw3-4 are controlling the second A32-range of PCI Base Register 4 and Page B.



The slave interface allows external access to the 512KB dual-port-RAM (DPR) via A24 or A32 modes.

The interface can operate in little- or big-endian-mode which allows the little-endian-x86 CPU to communicate with VME big-endian components without need to swap bytes in software.

The PCKV can also operate as system controller with its 4-level arbiter operating in round-robin-mode and supplying the 16MHz SysClock to the VME. As system-controller a Reset to the VME-Bus is generated.

The system controller mode is enabled by default and can be disabled by plugging a jumper on position J1.

Address-Modifiers (AM) 0x0D (A32), 0x3D (A24) and 0x2D (A16) are generated for master accesses. AM codes 0x0D, 0x09 (A32) and 0x3D, 0x39 (A24) are accepted for slave accesses to the DPR.

The VME interface operates internally at 80 MHz.

4.2 Dual-Port-RAM

The DPR can be accessed from the local PCI bus and the VME bus. It can be mapped to the VME in the A24 and/or the A32 address range. An arbitration logic grants simultaneous access from both buses.



5 Link

A fast 1.44Gbit serial connection using low-latency SerDes devices is used to transfer the access data from PCI to VME and read data, control messages and interrupt status from VME to PCI. To ensure a correct data transmission a 16 bit CRC is appended to all messages.

To maximize the performance write accesses are posted to VME and immediately acknowledged to the PCI. Therefore the next access can start on the PCI side while the previous access is still performed on the VME side. Further write accesses are collected in a FIFO on the VME side which can hold a maximum of 128 accesses.

Read accesses are delayed on the PCI side until all pending write accesses in the FIFO are executed, then the read access is performed and the data sent back to the PCI.

The Access-FIFO can be programmed with a low and high watermark. A „FIFO full“ control message is sent to the PCI side when the high watermark is reached and a „FIFO ready“ message when the low watermark is reached.

When the PCI side receives a „FIFO full“ message the next access is delayed until a „FIFO ready“ message is received.

The Link status can be observed in the Status Register. An interrupt is issued when the Link status changes.

When the VME side is disconnected or powered down the PCI interface will ignore any write data (the PCI access is still acknowledged as usual) and the read data returned is all '1' as if the VME access would be terminated with a Bus-Error.

The Link may be disconnected or either side be powered down and up at any time.

Whenever the Link is re-established it is automatically resynchronized and accesses are forwarded immediately to the VME side.

If the Link is interrupted and re-established while operating spurious CRC errors may be generated on both sides - this is not really an error. To check if an error occurred in normal operation the CRC error counter must be read after a successful connection and checked if the value changes.

5.1 Access FIFO Watermarks

The default watermarks for the FIFO are 4 (low) and 8 (high).

When the FIFO watermarks are programmed to other values the following conditions must be observed:

- the low mark must be lower than the high mark at any time
- the high mark must be below 126 to allow storing of the next access until the FIFO full message is transferred
- the low mark must be greater than 0

The difference between the low and the high watermark should not be very small or big, a small difference will lead to a lot of FIFO control messages from VME to PCI side, and a large difference will lead to frequent large delays on the PCI side. A difference of 4 is usually a good value for most applications.

The high watermark value should be about the largest number of write accesses which are issued by the application within a very short time, e.g. a block of data written in one go.



5.2 Link Test

The connection between PCI and VME can be tested in two ways: A static data test where a 16 bit test word is set and transmitted or an automatic Bit Error Rate Test where a pseudo random sequence is sent and checked on the remote side. Access to the remote registers is not possible in test mode, the only way to resume normal operation after starting the test is to reset the communication by setting the bit D7 in the Control Register (see 6.3.5). This will reset the VME registers to their default value and resume normal operation.



6 Register Description

All Registers can be read and written as byte, word or dword (32bit).

6.1 PCI Memory and I/O mappings

The PCI-VME-Bridge is PCI-Device No. 11 (0xB), using INTC# and having two Sub-Devices (Functions)

- Vendor-ID= 0x0EAC
- Device-ID= 0x000C
- Class-Code= 0x068000 (other Bridge-Device)
 - Base 0: I/O-Register (64B)
 - Base 1: VME A16 (64KB)
 - Base 2: VME A24 (16MB)
 - Base 3: VME A32 (256MB), Page A
 - Base 4: VME A32 (256MB), Page B

6.2 PCI Configuration Register

Offset	Register	Value
0x00	Device- & Vendor-ID	0x000C, 0x0EAC
0x04	Status & Command	
0x08	Class & Revision-ID	0x068000, 0x00
0x0C	BIST, Header, Latency, Cache	0x00, 0x80, 0x00, 0x00
0x10	Base 0	I/O-Register
0x14	Base 1	VME A16 (64KB)
0x18	Base 2	VME A24 (16MB)
0x1C	Base 3	VME A32 (256MB)
0x20	Base 4	VME A32 (256MB)
0x24	Base 5	not used
0x28	Cardbus CIS Pointer	0
0x2C	Subsystem Device- & Vendor-ID	0x000C, 0x0EAC
0x30	Expansion ROM	0
0x34	reserved	0
0x38	reserved	0
0x3C	MaxLat, MinGnt, IntPin, INT	0x00, 0x00, 0x01, IRQ



6.3 I/O-Register

Offset	Register	Value
x00	interface type	0x01010001
x04	FPGA firmware version	3
x08	Status	
x0C	reserved	0
x10	Interface and Link Configuration	
x14	Test Mode	
x18	Interrupt-Status/-Mask	
x1C	Control	
x20	VME-Page	
x24	uSec Counter	32bit microseconds counter
x28	Rx CRC Error Counter	32bit Counter, Receive errors
x2C	Tx CRC Error Counter	32bit Counter, CRC Error Messages
x30	Test-Mode Error Counter	32bit Counter
x34-3F	undefined/reserved	0

6.3.1 Status (0x08)

D20-31	Reserved (0)
D16-19	A32 Size Switch (see chapter 4.1)
D10-15	Reserved (0)
D9	1= Bus-Error, 0= last access OK
D8	1= CRC Error, 0= last access OK
D7-4	Reserved (0)
D3	1= remote card present/connected
D2	1= Link ready, 0= Syncing
D1	1= Link Up, 0= Link Down (Lock)
D0	1= VME Ready, 0= VME off/disconnected



6.3.2 Interface Config (0x10)

D31-18	Reserved (0)
D17-16	Transmitter Pre-Emphasis (0-3)
D15-10	Reserved (0)
D9-8	Receiver Equalization (0-3)
D7-4	Reserved (0)
D3	Enable Subtractive Decoding: 1= Enabled, 0= Disabled
D3-0	Reserved (0)

Default value: 0x0000.0100

The PCI subtractive decoding feature must not be activated by more than one device - use with care. Activating it might cause system failure and is therefore not recommended.

The advantage of using it is you can access the VME A32 space directly on all local addresses which are not used otherwise without need to map a portion into local address space.

6.3.3 Test Mode (0x14)

D31-16	Tx-Data
D15-0	Rx-Data

Default value: 0x0000.0000

6.3.4 Interrupt (0x18)

D31-30	0
D29-17	INT Mask for D13-1: 0= disabled 1= enabled
D16-15	0
D14	Global Interrupt pending bit (or of all other bits)
D13	Link Status changed
D12	0
D11	CRC Error
D10	Bus-Error
D9	PCI Parity Error
D8	0
D7-1	VME Interrupt
D0	PCI Interrupt Enable (1= Enable, 0= Disable)



Default value: 0x0000.0000
 D0-15 = Interrupt pending: 1= Active, 0= Inactive
 D16-31= Interrupt mask: 1= enabled, 0= disabled

6.3.5 Control (0x1C)

D31	1= Soft Reset
D30-25	Reserved (0)
D24	1= VME Access Enable (PCK Firmware V3)
D23-19	Reserved (0)
D18	SPI CSn (1)
D17	SPI Clock (0)
D16	SPI Din (rd) Dout (wr)
D15-8	Reserved (0)
D7	1= disable Link Ready signal to VME (Communication Reset)
D6-3	Reserved (0)
D2	1= BERT Test Mode
D1	1= Link Test Mode
D0	1= force Link Synchronisation

Default value: 0x0004.0000
 The SPI signals are for factory testing only, D18 MUST be written as '1' and D17 should always been written as '0' !.
 Bits 0-7 should be written as '0' for normal operation.
 Bit 24 must be set to '1' for normal operation, to enable accesses to the VME.
 Soft Reset: 1= assert Reset to the PCK logic.

6.3.6 VME Page (0x20)

D31-16	0
D15-8	VME A32 Page B
D7-0	VME A32 Page A

Default value: 0x0000.0000
 (see chapter 4.1)

6.3.7 uSec-Timer (0x24)

D31-0	Microseconds counter
-------	----------------------

6.3.8 CRC Error counter (0x28)

D31-0	Receiver CRC errors
-------	---------------------

CRC errors of VME messages received



6.3.9 VME CRC Error counter (0x2C)

D31-0	VME CRC errors
-------	----------------

CRC error control messages from VME side.

When the VME receiver has a CRC error it sends a „CRC error“ control message.

6.3.10 Test Mode Errors (0x30)

D31-0	Test data errors
-------	------------------

Error counter in link test or BERT mode.

6.4 VME Register

On the VME side there is an area of 1KB for the VME specific control registers mapped into the A24 address space.

The VME control field is set by the DIP-Switches to an address between 0xEA0000 and 0xEA7C00. As the slot is not known on the PCI card before reading the appropriate register, this area is also mapped at address 0xEAF800 on the local link. If multiple PCKV cards are located in the same rack each PCK card can reach its connected companion at this address.

- Slot 0: 0xEA0000 (Switch 5-1= 00000)
- Slot 1: 0xEA0400 (Switch 5-1= 00001)
-
- Slot 31: 0xEA7C00 (Switch 5-1= 11111)

Where a '1' means Switch=off, '0' means Switch=On

All registers can be read and written from the host (PCI side), they are read only on the VME bus except the “Link Configuration” bits 0-15 and “Link Status and Test” register at offset 0x50 and 0x58.



6.4.1 VME Control Register

Offset	Description
0-1	Card-ID = 0
2-3	Version = 0
4-5	VME Status
6-0xF	Reserved (0)
0x10-0x17	Product Name "PCKV "
0x18-0x1F	Reserved (0)
0x20-0x23	Company "SHF "
0x24-0x3F	Reserved (0)
0x40-0xDF	Control Register
0xE4-0xFF	Interrupt Acknowledge
0x100-0x3FF	RAM

6.4.2 VME Status Register (0x04)

D15	0
D14	SYSFAIL 0=active, 1=inactive
D13	0
D12	ACFAIL 0=active, 1=inactive
D11-8	0
D7	0= System Controller
D6-0	0



6.4.3 Interface Configuration (0x40)

D31-24	Arbiter time out in microseconds: 1-255
D23	1= enable VME A32 access to DPR
D22	1= DPR read only
D21-18	Reserved (0)
D17	1= Soft Reset
D16	1= enable VME A24 access to DPR
D15-8	Reserved (0)
D7	1= Big endian, 0= little endian mode
D6-5	Reserved (0)
D4	Arbiter mode: 1= round robin, 0= prioritised
D3	Reserved (0)
D2-1	Request Level: 0-3
D0	Enable VME to DPR access

Default value: 0x2000.0000

The arbiter time out must not be set to 0.

To enable access to the DPR from the VME bus two or three bits must be set: either D32 or D16 or both and D0.

6.4.4 DIP-Switch (0x47)

D31-24	DIP Switch, 1= Off, 0= On
--------	---------------------------

This is a Byte register, bytes at offset 0x44-46 are reserved.

6.4.5 DPR A32 Address (0x48)

D31-19	VME A31-19 base address of DPR
D18-0	Don't care (0)

Default value: 0x0000.0000

6.4.6 DPR A24 Address (0x4C)

D31-24	Don't care (0)
D23-19	VME A23-19 base address of DPR
D18-0	Don't care (0)

Default value: 0x0000.0000



6.4.7 Link Configuration (0x50)

D31	Reserved (0)
D30-24	Access-FIFO high watermark: 1-126
D23	Reserved (0)
D22-16	Access-FIFO low watermark: 1-124
D15-10	Reserved (0)
D9-8	Receiver Equalization (0-3)
D7-2	Reserved (0)
D1-0	Transmitter Pre-Emphasis (0-3)

Default value: 0x0804.0100

The Equalization and Pre-Emphasis should be set to 0 for testing purposes these bits can be written from the VME bus.

6.4.8 Microseconds Counter (0x54)

D31-0	Microseconds
-------	--------------

6.4.9 Link Status and Test (0x58)

D31-16	Write: Test Data, Read: Last control word received
D15	Link Reset, 1= Reset active
D14-11	Reserved (0)
D10	1= Link Ready (connected)
D9	1= Link Locked (synchronized)
D8	Host Ready, 1= Link Up, 0= Link down
D7-3	Reserved (0)
D2	1= Bit Error Rate Test (BERT)
D1	1= Link Test (send test data)
D0	1= force Link synchronization

Default value: 0x0000.0000

Bits 3-15 are read only

When the Link is up and operating bits 8-10 are all '1'.

This register can be written from the VME bus for testing purposes.

6.4.10 CRC Error Counter (0x5C)

D31-0	CRC receive errors
-------	--------------------



6.4.11 Test Error Counter (0x60)

D31-0	Receive errors in Link Test or BERT mode
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6.4.12 VME Error Register 1 (0x64)

When a VME Bus-Error occurs the bus status is sampled, the signals are stored with their real levels (0=low, 1=high):

D31-1	A31-1
D0	LWord

6.4.13 VME Error Register 2 (0x68)

D31-14	0
D13	Write
D12	IAck
D11-10	0
D9	DS1
D8	DS0
D7-6	0
D5-0	AM5-0

6.4.14 Access FIFO Error 0 (0x6C)

Internal Error register

D31-16	Erroneous control word
D15-0	Error counter

This is an internal test register. It should always be 0 in normal operation.

6.4.15 Access FIFO Error 1 (0x70)

D31-0	address
-------	---------

6.4.16 Access FIFO Error 2 (0x74)

D31-0	data
-------	------



6.4.17 Interrupt-Acknowledge (0xE4-0xFF)

A read access to these addresses issue an interrupt acknowledge access on the VME bus. PCI addresses A2-4 are output as A1-3 on the VME bus indicating which interrupt is to be acknowledged. Byte, word and dword accesses are possible, where byte accesses are only defined for the odd byte, the even byte is undefined. Write accesses to this area are ignored.

Byte access:

Offset	Acknowledged INT
0xE5	INT1
0xE9	INT2
0xED	INT3
0xF1	INT4
0xF5	INT5
0xF9	INT6
0xFD	INT7

For word and dword accesses use offsets 0xE4, 0xE8, 0xEC, 0xF0, 0xF4, 0xF8 and 0xFC. Word accesses to odd words (0xE6, 0xEA, ...) are undefined.

6.4.18 RAM (0x100-0x3FF)

This area is an additional fast real dual-port-RAM for data exchange.

7 Drivers

Drivers and application software examples for Linux 2.6 and Windows XP® are available including source code on the internet from our website: www.shf.de

(Windows and Windows XP are trademarks of Microsoft Corporation).



8 Technical Data

Cable: standard PCI Express 1x external up to 5 meters (15 feet)

8.1 PCK

Supply Voltage	Supply current typ.	Supply current max.
5V DC $\pm 5\%$	500 mA	700 mA
3.3V DV $\pm 5\%$	385 mA	570 mA

Power consumption: 3.8W typ., 5.4W max.

MTBF: 1415628h at 40°C (> 161 Years)

8.2 PCKV

Supply Voltage: 5V $\pm 5\%$

Supply current: 1.3A typ., 2.0A max.

Power consumption: 6.5W typ., 10W max.

(The max. values are given for typical operation on the VME bus, for worst case the max. supply current is 3A e.g. when writing zeros with Bus-Error abort).

MTBF: 580383h at 40°C (> 66 Years)

9 Environmental Conditions

Operating:

Temperature: 0 °- 55°C

Humidity: max. 10%-90% rel. (non-condensing)

(According to IEC 60068-2)

Vibration according to IEC 60068-2-6: max. 100 Hz, ± 1 mm

Storage:

Temperature: -20° - 85°C

Humidity: max. 95% rel. (non-condensing)

EMC and ESD compliant according EN 61000-4

ROHS compliant according WEEE 01-2003



10 Ordering Information

PCKP:	PCI card,	order no. 6001 100
PCKV:	VME card,	order no. 6001 110
PCK-1m:	1 meter cable,	order no. 6001 101
PCK-3m:	3 meter cable,	order no. 6001 103
PCK:	PCI-VME-Kit (PCKP+PCKV) with 3m cable, order no. 6001 120	

Other cable lengths on request.