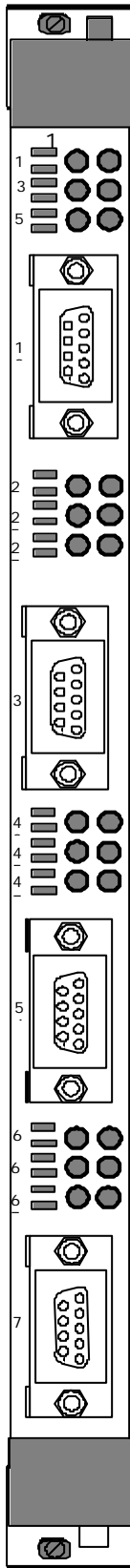


VME4SSI

Shaft-Angle Encoder Interface VME-Board

CONTENTS

| | |
|---------------------------------------|-----------|
| 1 General | 3 |
| 2 Functional Description | 3 |
| 2.1 Board Addressing | |
| 2.1.2 Base Address for VMEbus Subrack | 3 |
| 2.2 Address Modifier | 3 |
| 2.3 SSI Interfaces | 4 |
| 2.4 Possible Transducers | 5 |
| 2.5 SSI Data Transmission | 6 |
| 2.6 Position Detection | 7 |
| 2.7 Function Register | 8 |
| 2.8 Functional Control of the VME4SSI | 10 |
| 2.9 EMC Register | 10 |
| 3 Dialog Registers | 11 |
| 3.1 Command Register | 12 |
| 3.2 Acknowledgement Register | 12 |
| 3.3 Status Register | 12 |
| 3.4 Data Dialog Registers | 12 |
| 4 Connector Layout | 14 |
| 6 Assembly Diagram | 16 |
| 7 Connection Information | 17 |
| 8 Technical Specifications | 17 |



1. General

The VME4SSI input board measures the positions of up to four absolute transducers with an SSI interface (synchronous-serial interface). Single-turn, multi-turn shaft angle encoders and linear transducers - each with Gray or binary code - can be connected. The board does the necessary conversion from the Gray to the binary code. The front panel is fitted with the connector plugs for the shaft angle encoders and/or linear transducers and sockets, as well as LEDs for indicating the signal states. The VME4SSI is a plug-in-type VMEbus board of double Euroformat standard size (6 HEs - height units) with a width of 4 TE divisions

2. Functional Description

The board has 4 SSI channels (synchronous-serial data transmission from the transducer) with the clock pulse generators and data inputs allocated to the interfaces. All the channels are potential-isolated against each other and against the VMEbus. Each of the four channels measures and processes the position transmitted by the shaft-angle encoder or linear transducer, resp. In this context, conversion of Gray to binary code and evaluation of an optional transducer monitoring function (e.g. PFB power fail bit) are possible. The shaft-angle encoders and linear transducers are connected via 9-pin DSUB connectors on the front panel.

2.1 Board Addressing

The board has a VMEbus slave interface and uses an address area of 1 kByte in the A24:D16 address area. It is designed for use in standard VMEbus subracks. BERR* is output in the case of an access to the VME4SSI with A24:D16 and LWORD* active. The same applies to an attempt of writing into the identification register or into the position registers.

2.1.2 Base Address for VMEbus Subrack

The slot (location) address for generating the base address can be set on the VME4SSI internally on the VME4SSI by means of DIP switch S1.

The basic address is **ea0000 (can be customer set by SHF to other areas)**

Setting the slot (location) address:

ea0000

S1 - 1 ^2 0 ea0400

S1 - 2 ^2 1 ea0800

S1 - 3 ^2 2 ea1000

S1 - 4 ^2 3 ea4000

S1 - 5 ^2 4 ea8000

Position "ON" ^ 0-signal

 "OFF" ^ 1-signal

2.2 Address Modifier

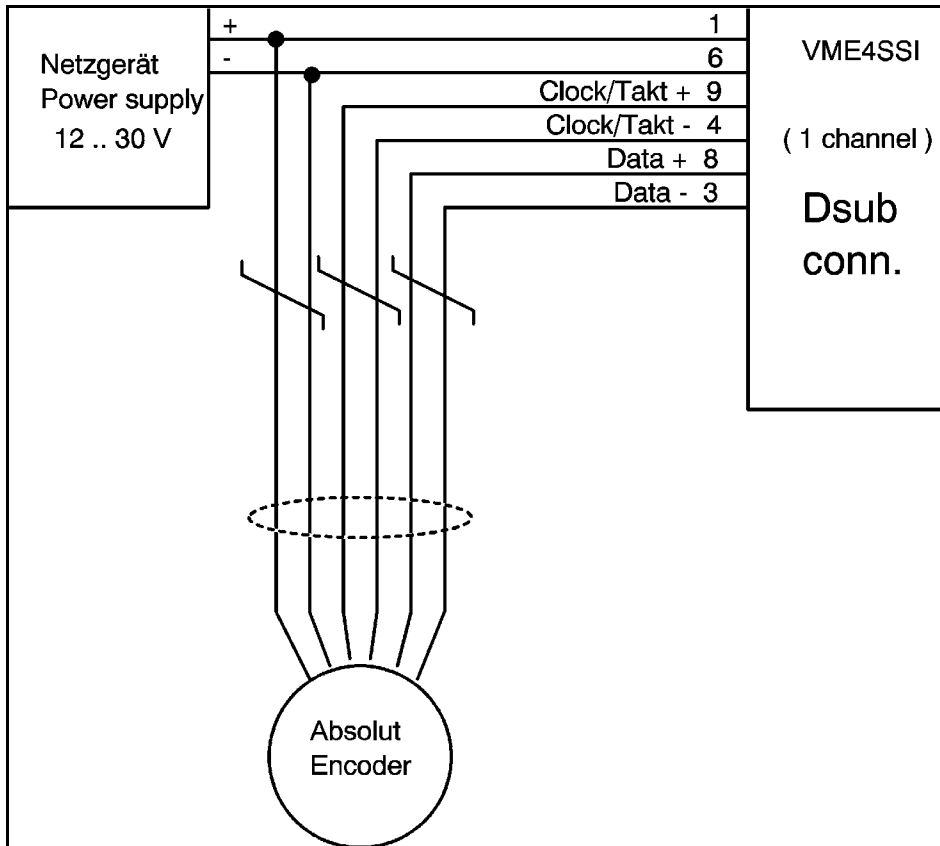
The VMESSI responds to user and supervisor accesses only with AM codes (AM0 ... AM5) for the A24:D16 area, with the possibility of presetting 39H or 3DH as AM codes..

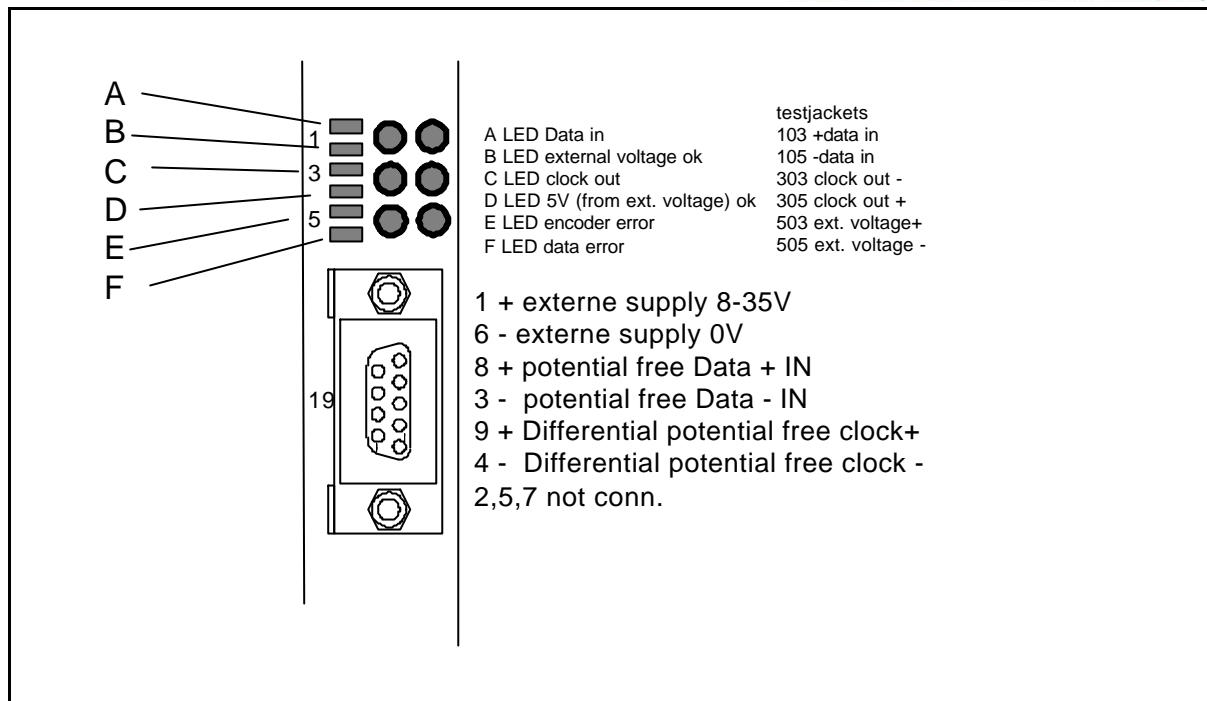
2.3 SSI Interfaces

The four SSI interfaces for connecting the shaft angle encoders and/or linear transducers have the following structure:

Example: transducer channel 0

VME4SSI





Note: It is absolutely essential that the periphery is connected properly because a wrong connection of the supply voltage can lead to the destruction of the interface circuits. Confounding of signal cables can cause loss of information. The measuring sockets on the front panel are connected through a resistor to the measuring signal.

2.4 Possible Transducers

Single-turn, multi-turn shaft angle encoders and linear transducers can be connected to the interfaces of the VME4SSI. Note that the VME4SSI supports only those transducers which transmit a data length of 13 or 25 bits, resp. and which have a certain data format (see para. 2.5). Absolute single-turn shaft angle encoders divide a mechanical revolution (0 to 360°) into a defined number of measuring steps which are repeated after one revolution. The resolution is normally 4096 steps (12 bits) or a maximum of 8192 steps (13 bits) in exceptional cases. Absolute multi-turn shaft angle encoders not only measure the angular position of a revolution, but also discriminate between several revolutions. The resolution is normally 4096 steps per revolution, multiplied by 4096 revolutions (24 bits), or a maximum of 8192 steps, multiplied by 4096 revolutions (25 bits), in exceptional cases.

Linear transducers transmit the absolute position. The precision depends on the length of the measuring distance and the data length of the transducer. Typical transducer resolutions are 12 or 24 bits and, in exceptional cases, 13 or 25 bits, resp.

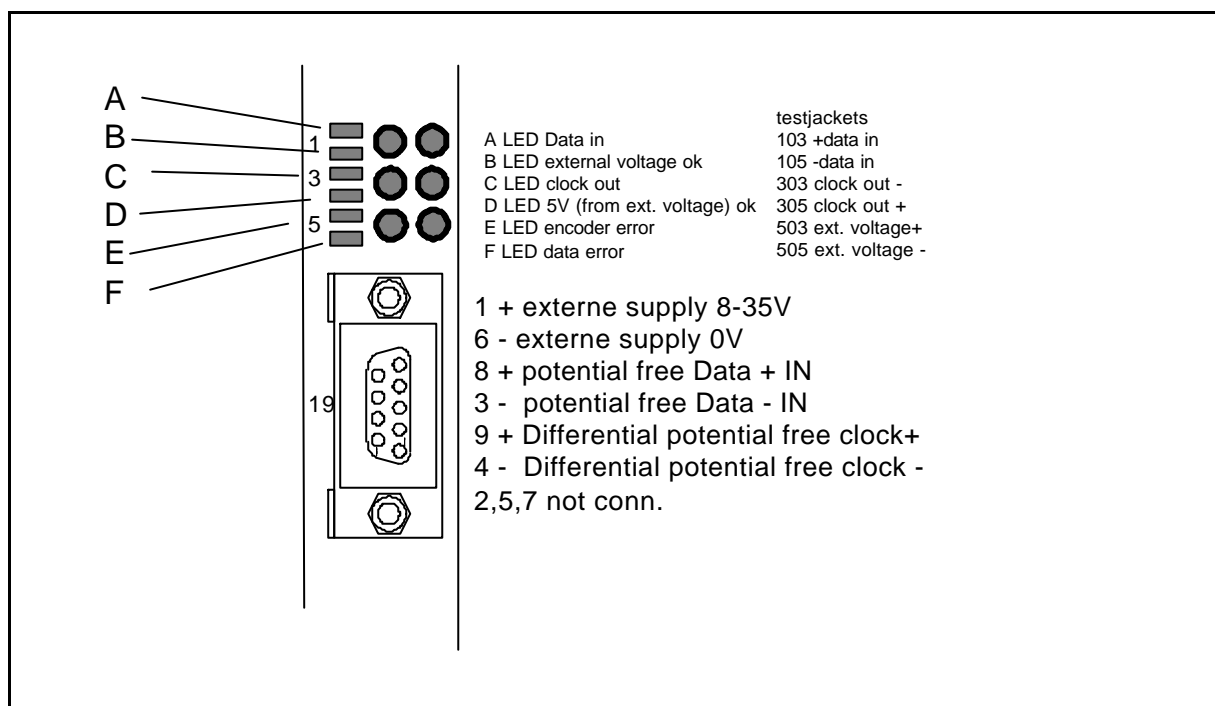
The VME4SSI supports shaft-angle encoders and linear transducers with binary and Gray code.

Shaft angle encoders and linear transducers transmit a data length of 13 or 25 bits, resp. All the bits are evaluated for identifying the position in exceptional cases only. The least significant bit (D0) is normally available for monitoring purposes only (e.g. PFB power fail bit), or is transmitted as a constant zero.

2.5 SSI Data Transmission

Shaft angle encoders and linear transducers with an SSI interface (synchronous-serial interface) and the data format described herein can be connected to the VME4SSI. The transducer position is supplied as a serial information which is synchronized with a clock pulse (i.e. a defined number of pulses) which is supplied by the VME4SSI. Transmission between transducer and VME4SSI (clock and data as serial position information) takes place via RS 422 interfaces with differential inputs and outputs. All the four transducer interfaces have the same structure and layout - even in terms of their connector layout - so that only one transducer interface is described here. The illustration shows the clock supplied by the VME4SSI and the information (position) supplied by the transducer. Note that the signals are symmetrical (RS 422).

The serial information supplied by the transducer is delayed by the time T_v ($T_v < 300$ ns) in relation to the positive clock edges fed into the transducer. The number of clock pulses supplied depends on the transducer type selected (13 or 25 bits, resp.). After the last clock edge, the "Data +" transducer output changes to a 1-signal after the time t_m ($t_m = 15 \dots 25 \mu s$)



Note: In the case of transducers with an outgoing cable, the shield is usually connected to the enclosure. The VME4SSI can be used to measure the position of transducers transmitting information with a data length of 13 or 25 bits. What is important in this context is that the most significant bit of the information is the first of the bits transmitted by the transducer. The total number (i.e. 13 or 25 bits, resp.) is completely used for the information in exceptional cases only. The transducer normally sends an optional monitoring bit (e.g. PFB power fail bit) or a constant zero as the last data bit.

The information supplied by a linear transducer is at the same time also the absolute position. In the case of a single-turn shaft angle encoder, the position of the transducer within one revolution is reported. In the case of a multi-turn shaft angle encoder, the upper 12 bits represent the number of revolutions, whilst the lower bits correspond to the position of the

transducer during the next revolution. The following illustration shows, as an example, the data format of a multi-turn shaft angle encoder supported by the VME4SSI. The resolution of this multi-turn shaft angle encoder totals 4096 revolutions with 4096 steps per revolution (4096 x 4096), and a monitoring bit (PFB power fail bit) is available also. The functionality of the monitoring bit can vary from transducer type to transducer type.

Clock + = Clock pulses supplied by the VME4SSI (valent output)

D0 .. D23 = Information 2 0 .. 2 23 (Gray or binary code).

PFB = In the event that the actual supply voltage remains below the minimum supply voltage by more than approx. 5V for more than 100µs, the data information from the transducer may be distorted. The power fail bit (PFB) identifies this error by a 1-signal

2.6 Position Detection

All the transducer channels have downstream position registers with an output to the VMEbus.

The position registers have a capacity of 32 bits. The utilization of the registers depends on the transducer type used. The VME4SSI supports transducers which transmit data lengths of 13 and 25 bits, resp. This means that either the data bits D0 to D12 (13 bits) or D0 to D24 (25 bits) are used for information. The remaining bits of the registers have a constant 0.

Contents of the position register of a 13-bit transducer:

D0 D15 **LOW word** D15-D12 =0

D16 D31 **HIGH word** all=0

Contents of the position register of a 25-bit transducer:

D0 D15 **LOW word**

D16 D31 **HIGH word** D31-D25 =0

Note: After receipt of all the data, the information sent by the transducer is loaded into the associated position register. In the case of a simultaneous receipt and reading of the output memory, data inconsistency is possible, particularly in the case of a 25-bit transducer (LOW word and HIGH word belonging to successive data receipts). It is hence recommended reading and comparing the values several times.

The data bits are weighted differently by the different manufacturers. The complete contents of the register are available for the position information in exceptional cases only. The least significant bit normally serves as an optional monitoring bit (e.g. PFB power fail bit), or a constant 0 is assigned to D0. This means that 12 or 24 bits, resp. are available for the position information. What is important is that the most significant bit of the information D12 or D24, resp. is the first of the bits transmitted by the transducer.

2.7 Function Register

For each transducer channel, a separate function register is available in the board. This function register is used for programming the function of the channel. In the event of a change in function, non-plausible output values can temporarily occur in the associated position register.

| Clock frequency | D10 | D9 | D8 |
|-----------------|-----|----|----|
| 1MHz | 0 | 0 | 0 |
| 500KHz | 0 | 0 | 1 |
| 250KHz | 0 | 1 | 0 |
| 125KHz | 0 | 1 | 1 |

data length

| | | |
|-----|---|--------|
| D11 | 1 | 25bits |
| D11 | 0 | 13bit |

Transducer PFB

| | | |
|-----|---|--------|
| D12 | 0 | no PFB |
| D12 | 1 | PFB |

coding

| | | |
|-----|---|-----------|
| D13 | 0 | binary |
| D13 | 1 | Gray-Code |

Report Power Fail Bit

| | | |
|-----|---|--------------|
| D14 | 0 | PFB not send |
| D14 | 1 | PFB send |

Report transducer error

D15 = 0,

Transducer supply available and data output of transducer properly connected.

D15 = 1,

Transducer supply not available, or permanent output of transducer improperly connected to VME4SSI data input.

The contents of D0 to D7 have no function (undefined contents).

D0-D7 no function

Explanation of function register contents:
- Clock frequency (D8 - D10)

The maximum permissible clock frequency mainly depends on the capacity of the cable between transducer and VME4SSI and hence on the length of the cable. In the case of a signal distortion of the transducer information, it must be ensured that the signal change of the transducer information takes place with a lead time of $t > 100\text{ns}$ before the next clock edge. The signal distortion can be measured at the measuring sockets of the VME4SSI. The following table illustrates the relationship between clock frequency and cable length:

| Cable length | Clock frequency | Reading time for a 13-bit transducer | Reading time for a 25-bit transducer |
|---------------------|------------------------|---|---|
| < 50 m | 1 MHz | < 20 ms | < 30 ms |
| < 100 m | 500 kHz | < 40 ms | < 60 ms |
| < 200 m | 250 kHz | < 80 ms | < 120 ms |
| < 400 m | 125 kHz | < 120 ms | < 240 ms |

- Transducer type (D11)

The transducer type (data length 13 or 25 bits) determines the number of clock pulses supplied by the VME4SSI.

- Transducer - power fail bit (PFB) (D12)

In the case of a transducer with a monitoring bit (e.g. PFB power fail bit), the selection of D12 = 1 means that the monitoring bit transmitted by the transducer is entered at D14 where it is then available for evaluation purposes.

- Transducer coding (D13)

With D13 = 1, the Gray code received is automatically converted to binary code and in this form stored in the position register. With D13 = 0, the Gray code received is directly stored in the position register.

D13 must be = 0 if a transducer with binary code is used. In the case of D13 = 1, the value stored in the position register is not defined.

- Power fail bit signal (PFB) (D14)

In the case of a transducer with a monitoring bit (e.g. PFB power fail bit) and selection of D12 = 1, this bit shows in the event of a PFB whether the supply voltage has remained below the transducer supply voltage by 5V for more than 100 μs , so that distortion of the transducer information is possible.

- Transducer error signal (D15)

This message indicates whether the transducer supply is available and whether the data output of the transducer is properly connected

2.8 Functional Control of the VME4SSI

The following functions can be determined via the command register (see para. 3.1):

-Start bit

After a SYSRESET* or connection of the supply voltage (UB5), the board is not ready for operation during the initialization phase only. Thereafter, the channels can be initialized, and the position registers can be read by the board.

The start bit serves for direct checking as to whether the VME4SSI can be addressed by the central unit.

- Asynchronous or synchronous operation

The VME4SSI can work in the asynchronous.

In the asynchronous mode, the position detecting function is free-wheeling, i.e. SSI data transmission is triggered continuously.

2.9 EMC Register

An EMC sensor on the board measures the electromagnetic alternating field to which the board is exposed. Level 1 responds in the case of fault level III as standardized in accordance with IEC 801-4 where the board still works in a reliable manner under laboratory conditions. This message, however, must already be regarded as a fault warning. Level 2 responds in the case of fault level IV as standardized in accordance with IEC 801-4 where the proper functioning of the board is no longer ensured. This message must be regarded as a fault message. Bit 6 and bit 7 in the status register (see para. 3.3) represent the degree of EMC exposure

3. Dialog Registers

The dialog with the VMEbus is handled via these registers, as follows:

| Base address | Access | Data size | Remarks |
|--------------|--------------|-----------|---|
| + 0 H | write only | 2 Byte | Command register, see para. 3.1 |
| + 2 H | read only | 2 Byte | Acknowledgement register, see para. 3.2 |
| + 4 H | read only | 2 Byte | Statusr register, see para. 3.3 |
| + 6 H | read only | 2 Byte | Error code register (0x0), here without any function |
| + 8 H | read only | 8 char | Identification, basic board type VME4SSI |
| + 10 H | read only | 8 char | Identification, board type VME4SSI |
| + 18 H | read only | 4 char | Identification, manufacturer SHF |
| + 26 H | read only | 2 char | Identification, revision code (0x0) |
| + 28 H | read only | 4 char | Identification, . date of manufacture, e.g. 0597 (5 th week 97) |
| + 34 H | read only | 8 char | Identification, firmware version (0x0) |
| + 3E H | read only | 2 Byte | Identification, free description (0x0) |
| + 80 H | read / write | 2 Byte | Function register for channel 0, see para. 2.7 |
| + 82 H | read / write | 2 Byte | Function register for channel 1, see para. 2.7 |
| + 84 H | read / write | 2 Byte | Function register for channel 2, see para. 2.7 |
| + 86 H | read / write | 2 Byte | Function register for channel 3, see para. 2.7 |
| + 100 H | read only | 2 Byte | Data dialog register: |
| .. | ... | ... | Position register for channels 0 ... 3 (see para. 3.4 |
| + 11E H | read only | 2 Byte | |

3.1 Command Register

The following functions are implemented in the command register:

| Bit No. | Description | Action | Remarks |
|---------|-------------------------|-------------|--|
| 4 | Ackn. of error messages | static | Reset bit 6 and bit 7 in the status register |
| 5 | Start bit | Edge 0 -> 1 | Set bit 5 in the acknowledgement register |

Explanations:

Bit 4 : Resetting the error memory by the software.

Bit 5 : See "start bit" (section 2.7).

SYSRESET* or power-on (UB5) resets bits 0 to 15 (0-signal) of the command register

3.2 Acknowledgement Register

The acknowledgement register contains acknowledgement information for the following bits of the command register:

| Bit No. | Description | Remarks |
|---------|-------------------------------|---|
| 4 | knowledgement of error essage | 1 = acknowlegement performed (see para. 3.1) |
| 5 | Start bit | 1 = after Start bit setting 0 = after SYSRESET or power-on |

3.3 Status Register

The status register of the VME4SSI contains the following messages:

| Bit No. | Description | Remarks |
|---------|--------------------|--|
| 0 | Initialization | 1 = Initialization underway 0 = Board initialization complete |
| 6 | EMC sensor warning | 1 = EMC level 1 exceeded 0 = ok. |
| 7 | EMC sensor warning | 1 = EMC level 2 exceeded 0 = ok. |
| 11 | VME accesses 1) | 1 = VME accesses t > 130 ms (timeout) 0 = accesses t < 130 ms |

1) Only applicable to accesses to the data dialog register (output memory)

3.4 Data Dialog Registers

These registers permit accesses to the position registers of the transducer channels (see para. 2.6):

| Base address | Description | Access | Size | Remarks |
|--------------|------------------------------|-----------|--------|----------------------------------|
| + 100 H | Position register, channel 0 | read only | 2 Byte | Low word |
| + 102 H | Position register,channel 0 | read only | 2 Byte | High word |
| + 104 H | Position register,channel 0 | read only | 2 Byte | Mirroring of <base address + 100 |
| + 106 H | Position register,channel 0 | read only | 2 Byte | Mirroring of <base address + 102 |
| + 108 H | Position register,channel 1 | read only | 2 Byte | Low word |
| + 10A H, | Position registerchannel 1 | read only | 2 Byte | High word |
| + 10C H | Position register,channel 1 | read only | 2 Byte | Mirroring of <base address + 108 |
| + 10E H | Position register,channel 1 | read only | 2 Byte | Mirroring of <base address + 10A |
| + 110 H | Position register,channel 2 | read only | 2 Byte | Low word |
| + 112 H | Position register,channel 2 | read only | 2 Byte | High word |
| + 114 H | Position register,channel 2 | read only | 2 Byte | Mirroring of <base address + 110 |
| + 116 H | Position register,channel 2 | read only | 2 Byte | Mirroring of <base address + 112 |
| + 118 H | Position register,channel 3 | read only | 2 Byte | Low word |
| + 11A H, | Position registerchannel 3 | read only | 2 Byte | High word |
| + 11C H | Position register,channel 3 | read only | 2 Byte | Mirroring of <base address + 118 |
| + 11E H | Position register,channel 3 | read only | 2 Byte | Mirroring of <base address + 11A |

The purpose of address mirroring is to ensure that both Big-Endian and Little-Endian processors can read such double words without swapping

4. Connector Layout

- VMEbus connector layout P1 (position X1)

| Pin No. | signalname | | |
|---------|------------|-----------|----------|
| | Row a | b | c |
| 1 | D00 | BBSY | D08 |
| 2 | D01 | BCLR | D09 |
| 3 | D02 | ACFAIL | D10 |
| 4 | D03 | BG0IN | D11 |
| 5 | D04 | BG0OUT | D12 |
| 6 | D05 | BG1IN | D13 |
| 7 | D06 | BG1OUT | D14 |
| 8 | D07 | BG2IN | D15 |
| 9 | GND | BG2OUT | GND |
| 10 | SYSCLK | BG3IN | SYSFAIL |
| 11 | GND | BG3OUT | BERR |
| 12 | DS1 | BR0 | SYSRESET |
| 13 | DS0 | BR1 | LWORD |
| 14 | WRITE | BR2 | AM5 |
| 15 | GND | BR3 | A23 |
| 16 | DTACK | AM0 | A22 |
| 17 | GND | AM1 | A21 |
| 18 | AS | AM2 | A20 |
| 19 | GND | AM3 | A19 |
| 20 | IACK | GND | A18 |
| 21 | IACKIN | SERCLK(1) | A17 |
| 22 | IACKOUT | SERDAT(1) | A16 |
| 23 | AM4 | GND | A15 |
| 24 | A07 | IRQ7 | A14 |
| 25 | A06 | IRQ6 | A13 |
| 26 | A05 | IRQ5 | A12 |
| 27 | A04 | IRQ4 | A11 |
| 28 | A03 | IRQ3 | A10 |
| 29 | A02 | IRQ2 | A09 |
| 30 | A01 | IRQ1 | A08 |
| 31 | -12V | +5V STDY | +12V |
| 32 | +5V | +5V | +5V |

P2 is only connected to VCC and GND, a19-a25 have to be left open!

- Periphery connector layout (positions X19, X35, X54, X75)

The shaft-angle encoders and linear transducers are connected via 9-pin DSUB plug connectors on the front panel.

| Connection | Meaning |
|-------------------|--------------------------|
| 1 | US (supply) |
| 2 | free |
| 3 | Data- (input) |
| 4 | Clock- (output) |
| 5 | free |
| 6 | MS (0 V) |
| 7 | free |
| 8 | Data+ (input) |
| 9 | Clock+ (output) |
| Enclosure | connected to front panel |

X19 ^ transducer channel 0

X35 ^ transducer channel 1

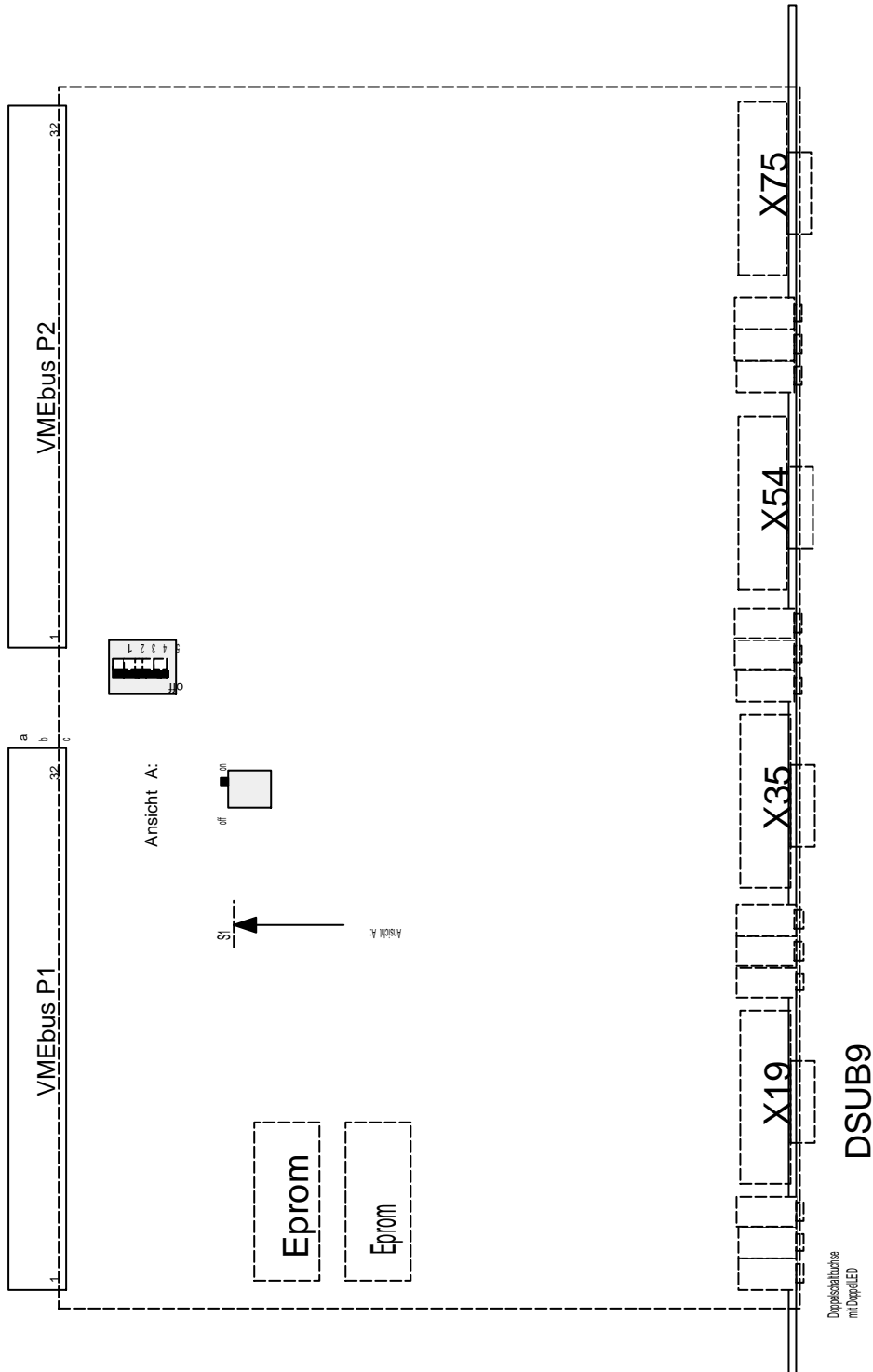
X54 ^ transducer channel 2

X75 ^ transducer channel 3

Note: It is absolutely essential that the periphery is connected properly because a wrong connection of the supply voltage can lead to the destruction of the interface circuits.

Confounding of signal cables can cause loss of information

VME4SSI



7.1 Connection Information

The connection of the transducers requires, for external wiring, cables with three twisted pairs and an overall screen, as follows:

- one twisted pair for Data + / Data --
- one twisted pair for Clock + / Clock --
- one twisted pair for the US / MS supply

The following cables are recommended:

- LifYCY 3x2 x0.20 mm 2 (manufacturer: Metrofunk)
- Unitronic-Bus FD-LD (article No. 2770215), manufacturer: Lappkabel, Stuttgart, Germany

The overall cable shield must be connected to the cubicle frame at the plug distributor with an all-over contact and with a low resistance.

Note: It is absolutely essential that the periphery is connected properly because a wrong connection of the supply voltage can lead to the destruction of the interface circuits. Confounding of signal cables can cause loss of information. When engineering the VME4SSI, make sure that the clock frequency for data transmission is appropriately parametrized, depending on the length of the cable between transducer and VME4SSI. The maximum clock frequency which can be selected also depends on the capacity of the cable between transducer and VME4SSI. It must be ensured that the signal change of the transducer information takes place with a lead time of $t > 100\text{ns}$ before the next clock edge supplied by the VME4SSI.

8. Technical Specifications

POWER SUPPLY

VMEbus processing UB5 = +5 V, $\pm 3\%$

I_{typ} < 500 mA

M5 = reference point (GND) for UB5

Periphery (transducer interface per channel)

Supply US = +24 V (12V.. 30V)

I < 50 mA (without SSI transducer supply)

MS = 0 V reference point for US

Inputs (Data+ / Data-) EIA RS422 potential-isolated against other channels and VMEbus

Insulation voltage U = 250 V AC

Outputs (Clock + / Clock-) EIA RS422 potential-isolated against other channels and VMEbus

Insulation voltage U = 250 V AC

AMBIENT CONDITIONS

Ambient temperature 0°C to +50°C (with natural convection)

Storage temperature -40°C to +80°C

Humidity class F

ELECTROMAGNETIC COMPATIBILITY

- Norm (pr) EN 50081-2 for interference emission
- Norm (pr) EN 50082-2 for interference immunity

MECHANICAL DESIGN

- **Format** INTERMAS Size 6 - 04

Dimensions approx. 233.4 mm x 160 mm x 20.5 mm (H x D x W)

- Connectors

VMEbus P1 E96M-C1A, connections X1 VMEbus P2 E64M-C1A, connections X2

Periphery 9-pin DSUB connectors (X19, X35, X54 and X75)

Weight approx. 400g