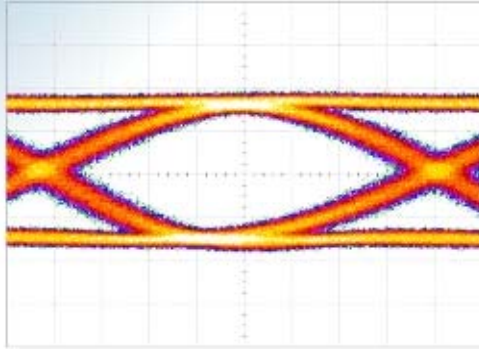




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# Datasheet

## SHF EA 44

### 44 Gbps Error Analyzer





## Description

The SHF EA 44 Error Analyzer is a tool for the detection of errors in gigabit transmission systems. Used in conjunction with the SHF BPG 44 or BPG 44 E Bit Pattern Generators, a system for bit error rate tests can be formed. Ease of use is ensured by simple hardware functions allowing phase adjustments or input threshold variations of the analyzer. It is therefore ideal for research and development of high speed logic MMICs and digital communications systems. Further applications include the testing of high rate PCM and SDH systems as well as digital optical components and sub-nanosecond pulse engineering.

Wideband operation from 2 to 44 Gbps simplifies testing, since the entire bandwidth can be easily accessed by altering the frequency of the clock signal. An input for an external clock generator is provided, and an internal fixed frequency low noise crystal oscillator clock is available as an option. As standard, the instrument operates at half-clock, so that the clock frequency is half that of the bit rate being analyzed. A full-clock version is also available. The phase shift between the clock and data signals can be adjusted using a computer controlled delay line, offering a delay of up to 160 ps, with a resolution of 1 ps. Error contours of constant error rate can be automatically measured by the instrument to aid setup and analysis.

A 4:1 44 GBit/s fast demultiplexer circuit reduces the input data stream to four signals, each with a rate of 11 GBit/s. The data is compared bit by bit to internally generated PRB sequences. Built in PRBS lengths are  $2^{31}-1$ ,  $2^{23}-1$ ,  $2^{15}-1$  or  $2^7-1$ . Errors are displayed for each channel as well as the total number of errors. Measurement intervals can be varied within the range  $10^6 \dots 10^{16}$  Bit/s.

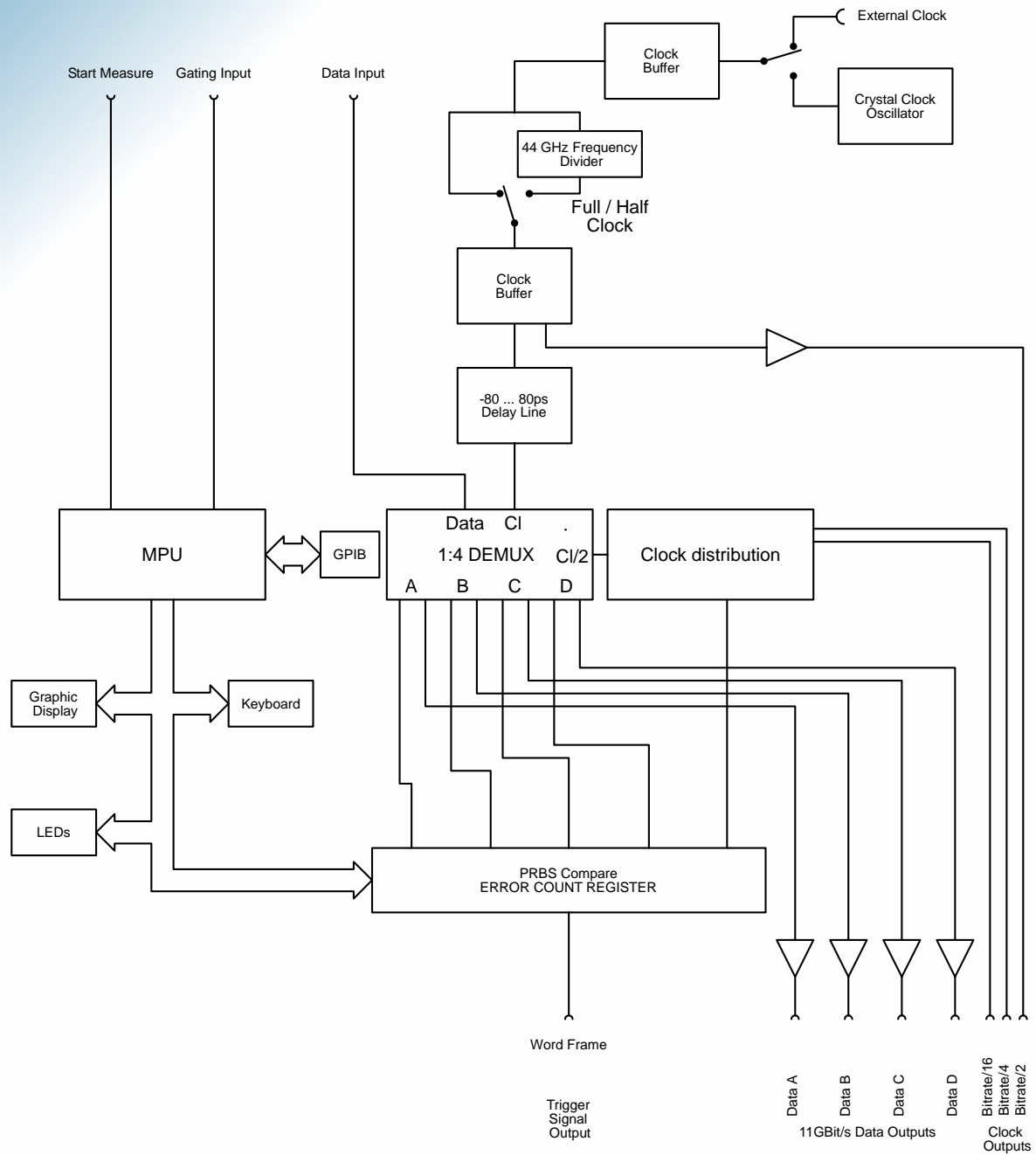
Word synchronization is achieved automatically, as indicated by four LEDs which light up when synchronization has been achieved. Shifting of sub-sequences is also tested, and a "MUX Error" is displayed if incorrect multiplexer interleaving is detected even though a single sub-sequence contains no errors.

## Features

- Handles CCITT-conforming PRBS patterns  $2^7-1$ ,  $2^{15}-1$ ,  $2^{23}-1$ ,  $2^{31}-1$
- Self-synchronizing, broadband operation
- Threshold adjustment by GPIB or manual thumbwheel
- MUX error indication
- Clock outputs at sub-harmonic rates
- Word frame output from internal 11 GBit/s channel A
- External clock input 22 GHz for BPG 40 A, BPG 44 or BPG 44 E compatibility
- Internal computer controlled 22 GHz timing delay line
- Display of total errors and the errors from each of the four 11 GBit/s sub-channels
- Full clock or half clock selectable
- Internal 6 digit true frequency counter displays the bit rate
- Measurement sequence start by TTL signal or push button
- Wide range of selectable gate times
- External GPIB control
- Low noise, low jitter timing circuits
- Burst Mode (fast synchronizing) capability



# Functional Block Diagram





# Specifications

Parameter	Unit	Min	Typ	Max	Conditions
Data input					AC coupled
Operating range	Gbps	2		44	
Phase adjustment	ps	0		160	1 ps step adjustment
Clock phase margin	°			200	see page 5
Bit pattern					$2^7-1, 2^{15}-1, 2^{23}-1, 2^{31}-1$
Sensitivity	mV <sub>pp</sub>			60	
Error counter Bit error rate		$10^{-2}$		$10^{-16}$	
Max. data input level <sup>1</sup>	V			1	NRZ, logic pos/neg selectable
S11	dB			-10	
Clock input <sup>2</sup>					AC coupled
Frequency range	GHz	1 2		22 44	half clock (standard) full clock (optional)
S11	dB			-10	
Input level	V <sub>pp</sub>	0.6		1	
Trigger outputs					AC coupled
Bitrate/N (N=2,4,16)/Wordframe	V <sub>pp</sub>	0.6	0.8	1.0	
S11	dB			-10	
Power supply	V	90 180	110 230	135 270	47...63 Hz
Power consumption	W		200		
Dimensions	mm				449x276x444
Weight	kg		20		
Operating temperature	°C	10		35	
Storage temperature	°C	-20		70	

<sup>1</sup> 1.85 mm ruggedized male connector

<sup>2</sup> 2.9 mm ruggedized male connector

## Clock output connectors:

Bitrate /2: 50 Ω ruggedized 2.9 mm precision male connector  
 Bitrate /4: 50 Ω ruggedized 2.9 mm precision male connector  
 Bitrate /16: 50 Ω SMA female connector

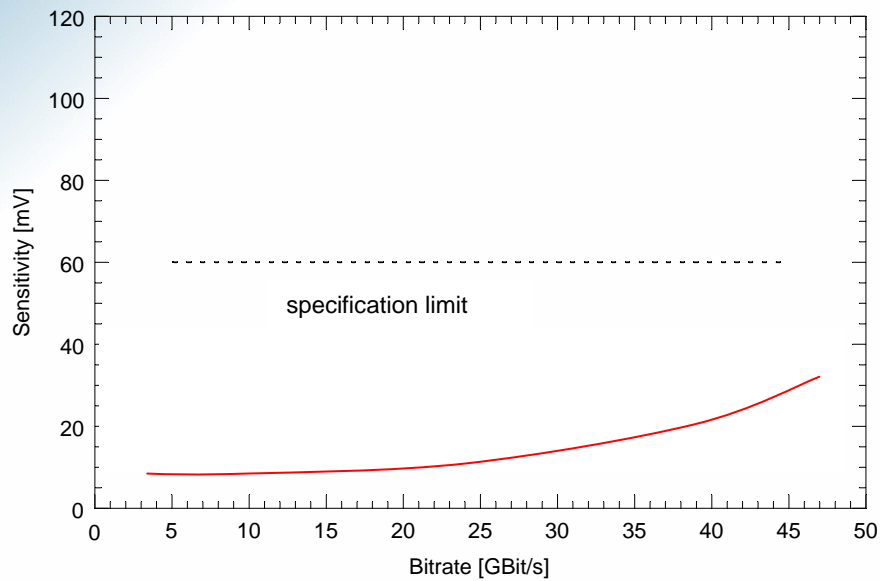
## Internal clock generator (Option 01)

60° C ovenized precision crystal oscillator  
 Available outputs: 1.244 GHz, 2.488 GHz, 4.976 GHz, 9.952 GHz, 19.904 GHz  
 (other frequencies, e.g. 21.5 GHz, available on request)  
 oscillator stability: < ± 1 ppm/° C;  
 warm up time: approx. 15 minutes;  
 ageing: < 3 x 10<sup>-9</sup>/d



## Test data

### Sensitivity

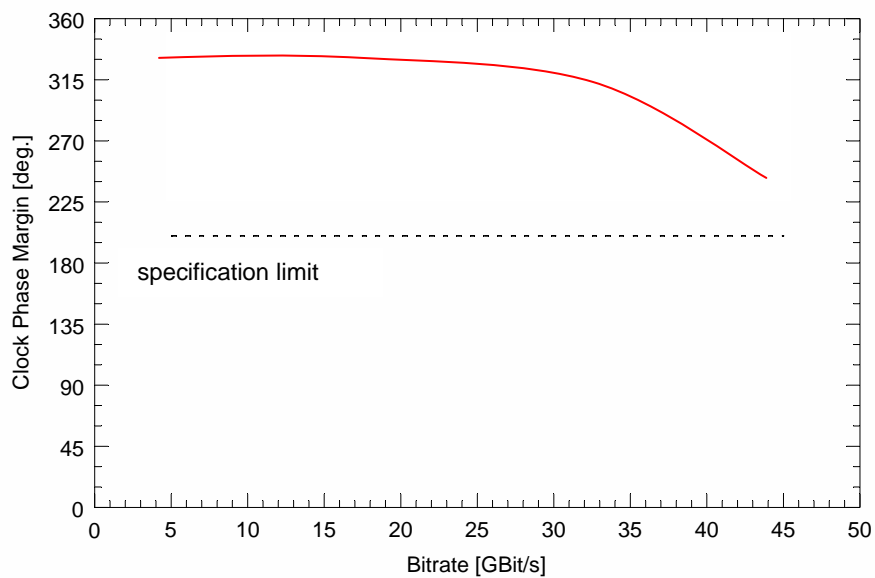


BER Limit  $10^{-9}$ , PRBS  $2^{31}-1$

Input signal attenuated with fixed attenuators until sensitivity limit was reached

Value shown corresponds to the measured eye height on an Agilent 86100 A Opt. 100 DSO

### Clock phase margin



BER Limit  $10^{-9}$ , PRBS  $2^{31}-1$ , Eye Height 100 mV, Peak-Peak-Source-Jitter 5 ps

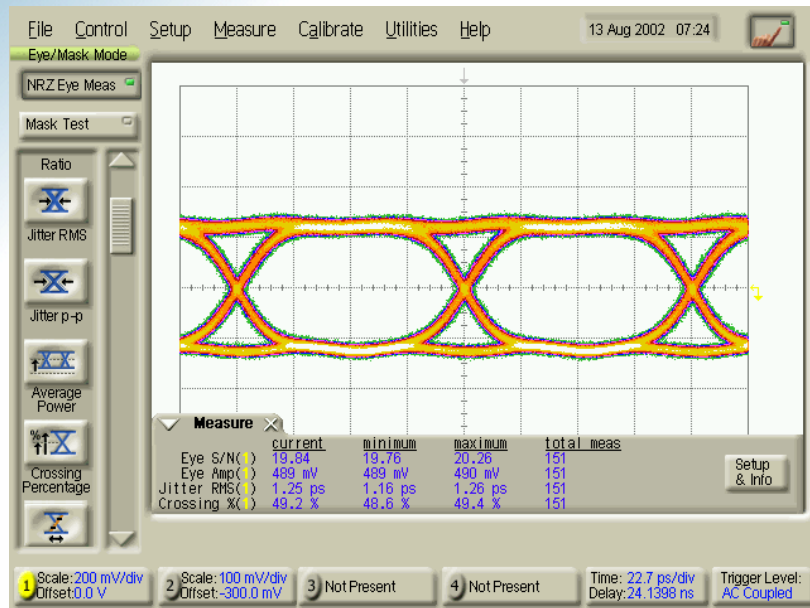
Peak-Peak-Source-Jitter as displayed on an Agilent 86100 A Opt. 100 DSO

Calculated using the formula:

$$\text{Clock Phase Margin [deg]} = \frac{\text{Phase Margin (measured) [ps]} + \text{Peak - Peak - Source - Jitter [ps]}}{\text{Eye Length [ps]}} \cdot 360^\circ$$



## Substrate output signal



PRBS  $2^{31}-1$

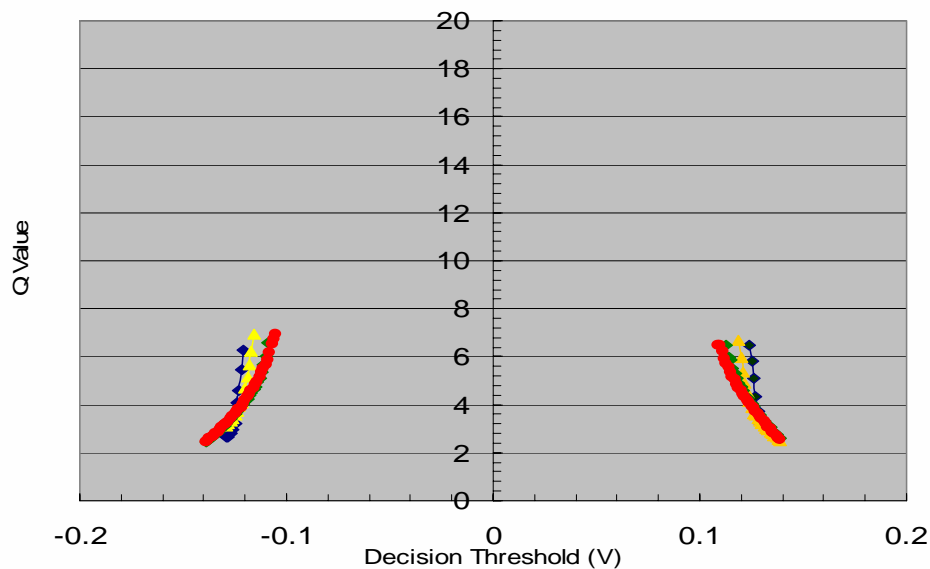
Input bitrate = 44 GBit/s

## Extrapolated Q-Factor

Taken from back to back measurements made in conjunction with the SHF BPG44 E Low Jitter error analyzer.

Q: 31 for  $2^{31}-1$ ; 95 for  $2^7-1$  prbs

Eye closure: < 13 % between  $2^7-1$  and  $2^{31}-1$  PRBS



Blue:  $2^7-1$

Yellow:  $2^{15}-1$

Green:  $2^{23}-1$

Red:  $2^{31}-1$